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EXAMINER

NADAV, ORI

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Please find below and/or attached an Office communication concerning this application or proceeding.

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DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 6, 11 and 14-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. The claimed limitation of a first sector having a narrower line width than a line width of the gate, as recited in claims 6, 11 and 15, is unclear as to what is meant by a line of a first sector and a line of the gate

4. The claimed limitation of a first surface region having a top surface and a bottom surface, wherein the top surface is larger than the bottom surface, as recited in claim 14, is unclear as to how a surface region can have a bottom surface.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 5-7 and 9-17, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian et al. (5,668,021) in view of Applicant Admitted Prior Art (AAPA).

Regarding claim 5, Subramanian et al. teach in figure 7 and related text a transistor comprising: a semiconductor substrate 10 of a first conductivity type; source and drain regions 28, 30, 34, 36 of a second conductivity type formed in the substrate and defining between them a channel region, an impurity implantation region 24 of impurities of a second conductivity type (column 3, lines 56-58) formed in a first sector of the channel region, the first sector (i.e. the region where the impurity implantation region 24 is located) not reaching either one of the source region and the drain region 28, 30, 34, 36, the impurity implantation region of the first sector comprising a depletion channel of the second conductivity type occupying a surface region of the semiconductor substrate, a second sector of the channel region exclusive of the first sector comprising an enhancement channel of the first conductivity type with uniform doping concentration and occupying a surface region of the semiconductor substrate, a gate insulating layer 12 on the substrate over at least a portion of the surface region of the first sector and the surface region of the second sector, and a gate 46 (14, 26 and 38, see column 5, lines 57-60) on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector.

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Although Subramanian et al. do not state that the second sector of the channel region comprises a uniform doping concentration, the embodiment of figure 7 does not recite any additional channel doping in the second sector (the second sector is a region in the channel region which is exclusive of the first sector) and no special substrate doping. Note that the second sector of the channel region is part of the substrate. Thus, the doping concentration of the substrate 10 is uniform, as claimed.

Subramanian et al. do not teach using the transistor as a pull up transistor, wherein one of the source and drain regions being electrically coupled to an I/O pad and the other one being electrically coupled to a Vdd terminal, and does not state that the impurity implantation region of the first sector is operable as a depletion channel, and the second sector of the channel region is operable as an enhancement channel.

AAPA teaches in figure 1 and related text (page 2, lines 1-15) a pull up transistor B, wherein one of the source and drain regions being electrically coupled to an I/O pad 20 and the other one being electrically coupled to a Vdd terminal.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Subramanian et al.'s transistor as a pull up transistor, wherein one of the source and drain regions being electrically coupled to an I/O pad and the other one being electrically coupled to a Vdd terminal, as taught by AAPA, in order to use the device in an application which requires a pull up transistor. Note that

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in order to operate a pull up transistor one of the source and drain regions must be electrically coupled to an I/O pad and the other one must electrically coupled to a Vdd terminal. The combination is motivated by the teachings of AAPA who point out the need for an improved pull up transistor.

Furthermore, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In this case, Subramanian's transistor is capable of performing as a pull up transistor.

Regarding the claimed limitations of an impurity implantation region of the first sector being operable under field effect as a depletion channel, and the second sector of the channel region being operable under field effect as an enhancement channel, although Subramanian et al. and AAPA do not state that the impurity implantation region of the first sector is operable under field effect as a depletion channel, and the second sector of the channel region is operable under field effect as an enhancement channel, these features are inherent in Subramanian et al. and AAPA's device for the following reasons. The first sector comprises first conductive type dopants and the second sector comprises second conductive type dopants. The equivalent circuit for Subramanian et al. and AAPA's transistor is identical to the equivalent circuit for

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applicant's transistor depicted in applicant's figure 7c. The equivalent circuit comprises three transistors operating at two different modes, a first sector operates at an n-channel (Subramanian et al., column 3, lines 59-61) as a depletion transistor, and a second sector operates at a p-channel as an enhancement transistor. Therefore, while operating the transistor as a pull up transistor, the impurity implantation region of the first sector of Subramanian et al. and AAPA's transistor is operable under field effect as a depletion channel (due to the first conductive type dopants), and the second sector of the channel region is operable under field effect as an enhancement channel (due to the second conductive type dopants), as claimed.

In the alternative, *regarding the claimed limitations of an impurity implantation region of the first sector being as a depletion channel, and the second sector of the channel region being as an enhancement channel, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function.* *In re Danley*, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does ."(emphasis in original) *Hewlett - Packard Co . v. Bausch & Lomb Inc .*, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). In this case, the claimed structure is not distinct from

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prior art's structure, because Subramanian et al. and AAPA's transistor is identical to applicant's transistor.

Regarding claim 10, Subramanian et al. teach an impurity implantation region having a lateral extent coextensive with the first sector, and occupying the entire top surface of the semiconductor substrate within the first sector.

Regarding claim 14, Subramanian et al. teach a first surface region having a top surface and a bottom surface, wherein the top surface is larger than the bottom surface.

Regarding claims 6, 11 and 15, Subramanian et al. teach in figure 7 and related text a first sector 24 having a narrower line width than a line width of the gate 46 (14, 26 and 38, see column 5, lines 57-60).

Regarding claims 7, 12 and 16, Subramanian et al. teach in figure 7 and related text a gate 46 (14, 26 and 38, see column 5, lines 57-60) comprises a first portion over the first sector and a second portion over the second sector; and the first portion is in a predetermined ratio with respect to the second portion.

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Regarding claims 9, 13 and 17, Subramanian et al. teach in figure 7 and related text a first sector separated from the source region and from the drain region by substantially equal distances (column 2, lines 45-47).

Response to Arguments

7. Applicant argues on page 6 that although figure 7 of Subramanian et al. depicts the top surface of region 24 being in direct contact with the surface of the substrate, the figures are not drawn to scale, and the surface region can be spaced away from the surface of the substrate.

Although figures are not necessarily drawn to scale, the illustration that the top surface of region 24 is in direct contact with the surface of the substrate is not related to the possibility that the figures may not be drawn to scale. Even if the figures are not drawn to scale, reducing or increasing the scale of the figure would not change the illustration that the top surface of region 24 is in direct contact with the surface of the substrate.

8. Applicant argues on page 7 that Subramanian et al. teach that the peak dopant concentration of buried region 24 is placed just below the surface of the substrate, and since region 24 is egg shaped, the topmost surface of region 24 must also lie just below the surface of the substrate.

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The location of the peak dopant concentration of buried region 24 just below the surface of the substrate, is not an indicator that the location of the topmost surface of buried region 24 is just below the surface of the substrate. On contraire, under normal doping conditions, the peak dopant concentration of a buried region is not located at the topmost surface of the buried region, but rather spaced from the boundaries of the buried region.

9. Applicant argues on page 8 that Subramanian et al. teach that buried region 24 is spaced away from the surface of the substrate, because the device of figure 7 combines the advantages of both surface and buried channel devices.

The examiner agrees that region 24 is a buried region, and thus the device of figure 7 has the advantages of both surface and buried channel devices. The fact that the top surface of buried region 24 is in direct contact with the surface of the substrate does not minimize the advantages that buried region 24 provides the device.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such

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papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is (703) 308-8138. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at (703) 308-2772.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is 308-0956



O.N.
May 12, 2003

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